

# Atomically Thin Indium-Tin-Oxide Transistors Enabled by Atomic Layer Deposition

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**Abstract**—In this work, indium-tin-oxide (ITO) transistors with atomically thin channel thickness ( $T_{\text{ch}}$ ) of 2.1 nm realized by atomic layer deposition (ALD) are demonstrated. A maximum ON-state current of 970 mA/mm at  $V_{\text{DS}}$  of 0.8 V and an ON/OFF ratio up to  $10^7$  are achieved in ITO transistor with In:Sn ratio of 9:1, channel length ( $L_{\text{ch}}$ ) of 60 nm, and dielectric equivalent oxide thickness (EOT) of 2.1 nm. Comparison between devices with different In:Sn ratios indicates a significant reduction of electron transport resulting from more Sn concentrations in ITO. The impact of back-end-of-line (BEOL) compatible low-temperature annealing is also investigated. An enhancement-mode operation with minimum subthreshold slope (SS) of 80 mV/dec and maximum field-effect mobility ( $\mu_{\text{FE}}$ ) of 28  $\text{cm}^2/\text{V}\cdot\text{s}$  is achieved after  $\text{O}_2$  annealing. Besides, bias instability measurement shows the negative threshold voltage ( $V_T$ ) shift under both positive and negative gate bias stress due to donor-like interface states below the trap neutral level (TNL). The realization of large-area synthesis of atomically thin ITO films by ALD and decent electrical performance provide opportunities in future monolithic 3-D device integration with BEOL compatibility.

**Index Terms**—Atomic layer deposition (ALD), back-end-of-line (BEOL) compatible, bias instability, indium tin oxide, low-temperature annealing, thin-film transistor.

## I. INTRODUCTION

THIN-FILM transistors (TFTs) based on amorphous oxide semiconductors have gained continuous attention over the past decades [1]–[7]. Due to several remarkable features, such as high carrier mobility, fast response, flexible ultrathin body, high transparency, amorphous oxide semiconductors are considered as competitive channel material candidates for

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next-generation BEOL-compatible CMOS transistor channels for monolithic 3-D integration [8]–[13]. However, the main challenges for the application of such materials so far are controllable large-scale ultrathin film synthesis as well as reliable device performance. ITO, as a wide bandgap oxide semiconductor (3.5–4.3 eV), is known to be widely used as transparent electrodes in optoelectronics, while its semiconductor behavior has been rarely explored due to its degeneracy in the conduction band. A high electron density for typical ITO is usually around  $10^{20}$ – $10^{21}/\text{cm}^3$ , leading to unsatisfactory switching characteristics [14]–[16]. By reducing the film thickness to modulate the bandgap and adjust the carrier density in oxide semiconductor materials as reported previously [14], [16]–[18], a functional ITO channel can be expected to meet the requirement for monolithic 3-D integration. ALD provides the unprecedented advantage to control the thickness and In:Sn ratio at the atomic accuracy compared to other physical vapor deposition (PVD) techniques.

In this article, the synthesis of ITO films with a thickness of 2.1 nm is realized by the ALD technique. High-performance ITO transistors with different In:Sn ratios, channel length ( $L_{\text{ch}}$ ) down to 60 nm, and channel thickness ( $T_{\text{ch}}$ ) of 2.1 nm are achieved with a maximum drain current of 970 mA/mm at a drain-to-source voltage ( $V_{\text{DS}}$ ) of 0.8 V and an ON/OFF ratio up to  $10^7$ . Comparison between ITO transistors with different Sn concentrations demonstrates that the electron transport in ALD ITO films is impeded by  $\text{SnO}_2$ , supported by density-functional-theory (DFT) simulation and modeling. The impact of BEOL-compatible low-temperature annealing in  $\text{O}_2$  and forming gas (FG, 96%  $\text{N}_2$ /4%  $\text{H}_2$ ) is also systematically studied.  $\text{O}_2$  annealing is found to shift the threshold voltage ( $V_T$ ) positively and an enhancement-mode operation with  $V_T$  of 0.33 V is observed in the ITO transistor with In:Sn of 9:1 and  $L_{\text{ch}}$  of 60 nm, which can be understood by the passivation of oxygen vacancies in the as-grown channel. In addition, bias instability measurement points out the possible existence of donor-like interface states below the trap neutral level (TNL), contributing to a negative  $V_T$  shift under stress.

## II. EXPERIMENTAL AND COMPUTATIONAL PROCEDURE

Fig. 1(a) illustrates the schematic of an ITO transistor. The gate-stack includes 40 nm Ni as the bottom gate, 5 nm  $\text{HfO}_2$  as the gate dielectric, 2.1 nm ITO as the semiconducting channel, and 60 nm Ni as source/drain contacts. Fig. 1(b) presents the fabrication process flow. Fig. 1(c) shows the scanning electron

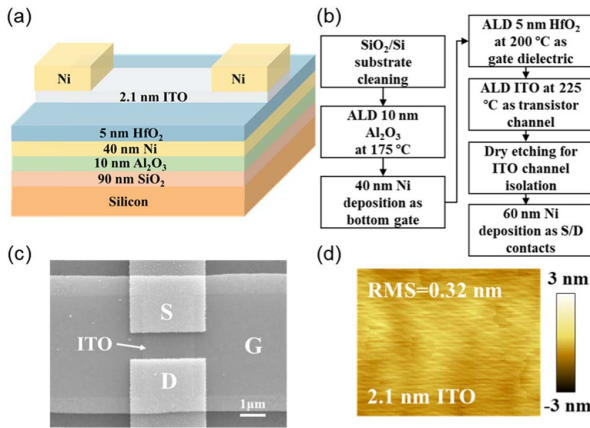


Fig. 1. (a) Schematic of the atomically thin ITO transistor with 40 nm Ni as the bottom gate. (b) Fabrication process flow of an ITO transistor. (c) SEM image of an ITO transistor with  $L_{ch}$  of 1  $\mu\text{m}$ . (d) AFM measurement of the surface roughness on a 2.1 nm as-grown ITO film with In:Sn ratio of 9:1.

microscopy (SEM) image of a typical fabricated ITO transistor with  $L_{ch}$  of 1  $\mu\text{m}$ .

The device fabrication process started with a standard cleaning process of  $p^+$  Si substrate with 90 nm thermally grown  $\text{SiO}_2$ . A standard cleaning process refers to that the substrate was rinsed with toluene, acetone, and IPA in an ultrasonic cleaner and dried by nitrogen to remove possible organic particles and dirty materials. A 10 nm  $\text{Al}_2\text{O}_3$  was deposited by ALD at 175  $^\circ\text{C}$  to obtain a smooth surface, using  $(\text{CH}_3)_3\text{Al}$  (TMA) and  $\text{H}_2\text{O}$  as Al and O precursors. A bilayer photoresist lithography process similar to [13] was then applied for the sharp lift-off 40 nm Ni bottom gate by e-beam evaporation. A 5 nm  $\text{HfO}_2$  was deposited by ALD at 200  $^\circ\text{C}$ , using  $[(\text{CH}_3)_2\text{N}]_4\text{Hf}$  (TDMAHf) and  $\text{H}_2\text{O}$  as Hf and O precursors. A 2.1 nm ITO was deposited by ALD at 225  $^\circ\text{C}$  with  $(\text{CH}_3)_3\text{In}$  (TMIn),  $[(\text{CH}_3)_2\text{N}]_4\text{Sn}$  (TDMASn), and  $\text{H}_2\text{O}$  as In, Sn and O precursors. TMIn and TDMASn precursors were heated to 60  $^\circ\text{C}$  to provide sufficient vapor pressure and  $\text{N}_2$  with a flow rate of 40 sccm was used as the carrier gas. The  $\text{HfO}_2$  and ITO were grown in two different ALD chambers but the two ALD systems are located in the same glovebox under environment control like a cluster system. This ALD process started with one cycle of  $\text{SnO}_2$  with TDMASn and  $\text{H}_2\text{O}$  pulsed for 2 and 1 s, respectively, followed by N cycles of  $\text{In}_2\text{O}_3$  with TMIn and  $\text{H}_2\text{O}$  pulsed for 0.625 and 0.75 s at each cycle, then repeated. N was set to 3, 6, and 9 to obtain ITO films with different In:Sn ratios. The thickness of the ALD ITO film was measured by ellipsometer (Gaertner L116A) and calibrated by transmission electron microscopy (TEM) and atomic force microscope (AFM). Fig. 1(d) shows a low surface roughness of 0.32 nm for the ITO film with In:Sn of 9:1 measured by AFM. No obvious difference of surface roughness is observed between ALD-deposited ITO films with different In:Sn ratios and before/after  $\text{O}_2$  annealing. ITO channel isolation was done by plasma dry etching ( $\text{BCl}_3$ : 15 sccm; Ar: 60 sccm; pressure: 0.6 Pa; RF source power: 100 W; RF bias power: 50 W; time: 20 s). 60 nm Ni was deposited by e-beam evaporation as source/drain contacts, patterned by electron beam lithography with  $L_{ch}$  ranging from 60 nm to 1  $\mu\text{m}$ . The fabricated devices

were also annealed in  $\text{O}_2$  and FG at 250  $^\circ\text{C}$  and 300  $^\circ\text{C}$  for 60 s to investigate the intrinsic properties of ALD ITO films.

The charge neutrality levels (CNLs) and band alignment of  $\text{In}_2\text{O}_3$  and  $\text{SnO}_2$  were calculated by DFT as implemented in the Vienna *ab initio* simulation package (VASP) [19], [20]. Perdew–Burke–Ernzerhof-generalized gradient approximation (GGA-PBE) functional is used for electron exchange-correlation interaction [21], [22]. The CNLs were calculated by performing Brillouin zone average using Kohn–Sham eigenenergies computed at  $\Gamma$ -centered Monkhorst–Pack  $k$ -points [23]

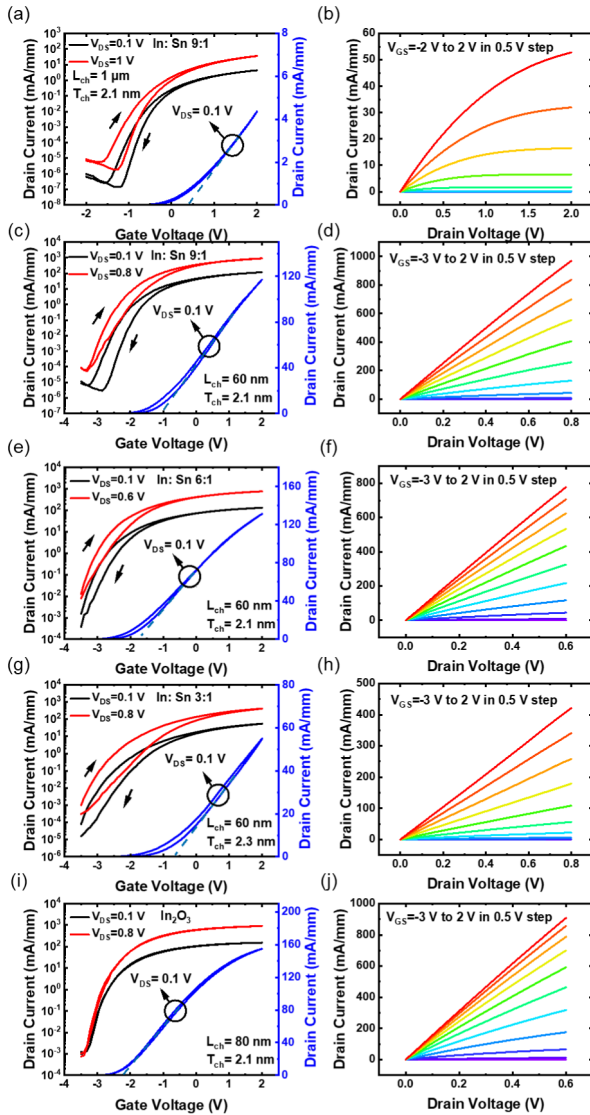
$$E_{\text{CNL}} = \frac{1}{2N_k} \sum_{k \in \text{BZ}} \left[ \frac{1}{N_{\text{CB}}} \sum_i^{N_{\text{CB}}} E_{\text{CB}_i}(k) + \frac{1}{N_{\text{VB}}} \sum_j^{N_{\text{VB}}} E_{\text{VB}_j}(k) \right]$$

where  $N_k$  is the number of  $k$ -points. For  $\text{SnO}_2$  unit cell containing two formula units, two conduction bands ( $N_{\text{CB}} = 2$ ) and four valence bands ( $N_{\text{VB}} = 4$ ) were used; for  $\text{In}_2\text{O}_3$  primitive cell containing eight formula units,  $N_{\text{CB}} = 16$  and  $N_{\text{VB}} = 32$ . The band alignment of  $\text{In}_2\text{O}_3$  and  $\text{SnO}_2$  was then determined by aligning their CNLs with valence band edges rigidly shifted to reproduce the experimental band gaps.

### III. RESULTS AND DISCUSSION

Fig. 2(a) and (b) show the transfer and output characteristics of an ITO transistor with In:Sn ratio of 9:1,  $L_{ch}$  of 1  $\mu\text{m}$  and  $T_{ch}$  of 2.1 nm. Decent drain current saturation is observed at high  $V_{\text{DS}}$  up to 2 V. A low contact resistance ( $R_C$ ) of 0.6  $\Omega\text{-mm}$  is extracted through the TLM method. Significant improvement of drain current can be achieved by channel length scaling. A maximum ON-state current of 970 mA/mm and an on/off ratio up to  $10^7$  are achieved at  $V_{\text{DS}} = 0.8$  V for a scaled device with  $L_{ch}$  of 60 nm as shown in Fig. 2(c) and (d). Fig. 2(e)–(j) present similar transfer and output characteristics of scaled ITO transistors with In:Sn ratio of 6:1 and 3:1, as well as pure  $\text{In}_2\text{O}_3$  transistors as the comparison group. Note that the hysteresis of the transfer curve is increasing from 0.14 V for In:Sn 9:1 device to 0.31 V for In:Sn 3:1 device, while a negligible hysteresis of 0.01 V is observed in pure  $\text{In}_2\text{O}_3$  transistor, suggesting such hysteresis may origin from the traps at the  $\text{In}_2\text{O}_3/\text{SnO}_2$  interface in ITO alloy formed during ALD growth.

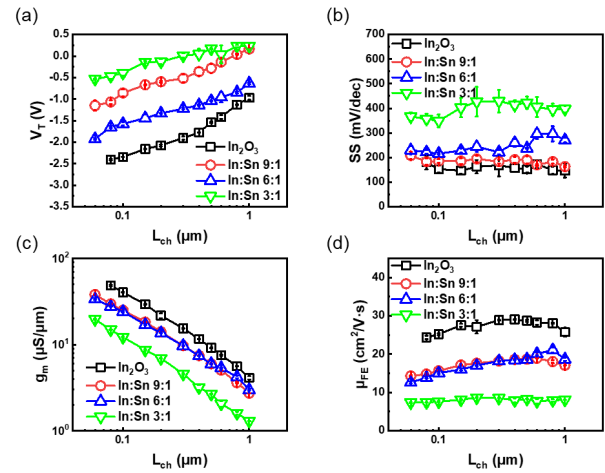
Fig. 3 summarizes the scaling metrics of ITO transistors with different In:Sn ratios and  $L_{ch}$  from 60 nm to 1  $\mu\text{m}$ . All parameters are extracted at  $V_{\text{DS}}$  of 0.1 V to avoid the impact of the self-heating effect. Each data point represents the average of at least three devices. The small error bar indicates the ultrathin ITO films grown by ALD are highly uniform at least in the area of 1  $\text{cm}^2$  sample size. Fig. 3(a) shows In:Sn ratio-dependent  $V_T$  relation. A trend of positive  $V_T$  shift is demonstrated as Sn concentration increases. Fig. 3(b) and (d) present the In:Sn ratio-dependent subthreshold slope (SS) and field-effect mobility ( $\mu_{\text{FE}}$ ) versus  $L_{ch}$  characteristics. A minimum SS of 163 mV/dec and a maximum  $\mu_{\text{FE}}$  of 19  $\text{cm}^2/\text{V}\cdot\text{s}$  are achieved in the ITO transistor with In:Sn ratio of 9:1 and  $T_{ch}$  of 2.1 nm. The threshold voltage ( $V_T$ ) was extracted by the linear-extrapolation method at  $V_{\text{DS}} = 0.1$  V. SS was the average value over several decades in the subthreshold region.



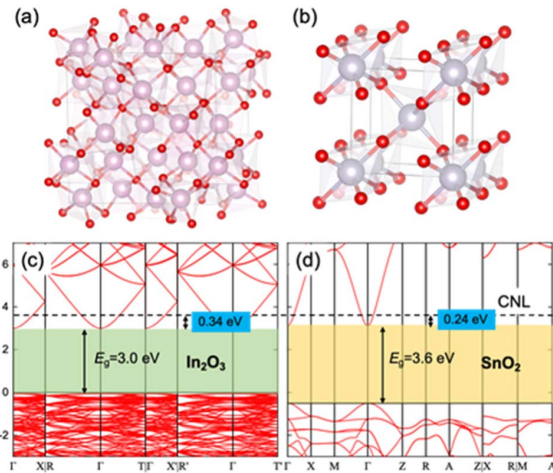
**Fig. 2.** (a) Transfer and (b) output characteristics of an ITO transistor with In:Sn ratio of 9:1,  $L_{ch}$  of 1  $\mu\text{m}$ , and  $T_{ch}$  of 2.1 nm. (c) Transfer and (d) output characteristics of an ITO transistor with In:Sn ratio of 9:1,  $L_{ch}$  of 60 nm, and  $T_{ch}$  of 2.1 nm. (e) Transfer and (f) output characteristics of an ITO transistor with In:Sn ratio of 6:1,  $L_{ch}$  of 60 nm, and  $T_{ch}$  of 2.1 nm. (g) Transfer and (h) output characteristics of an ITO transistor with In:Sn ratio of 3:1,  $L_{ch}$  of 60 nm, and  $T_{ch}$  of 2.3 nm. (i) Transfer and (j) output characteristics of an  $\text{In}_2\text{O}_3$  transistor with  $L_{ch}$  of 80 nm and  $T_{ch}$  of 2.1 nm.

The  $g_m$  was measured at  $V_{DS} = 0.1$  V and also the average value. All  $\mu_{FE}$  were calculated at  $V_{DS} = 0.1$  V. Besides, it can be seen that SS increases and  $\mu_{FE}$  decreases with more Sn doping concentration in ALD ITO films.

To understand such In:Sn ratio-dependent device performance, DFT calculation was performed to determine the band alignment between  $\text{In}_2\text{O}_3$  and  $\text{SnO}_2$  as shown in Fig. 4. The presence of the interfaces and amorphous disorders in ALD films pins the Fermi level at the CNL. The band edges of  $\text{In}_2\text{O}_3$  and  $\text{SnO}_2$  are therefore positioned by aligning their CNLs to ensure the Fermi level stays continuously throughout the heterointerface [23]. For both  $\text{In}_2\text{O}_3$  and  $\text{SnO}_2$ , their CNLs lie above the conduction band edges (CBE). Note that the calculated CNL of  $\text{In}_2\text{O}_3$  (0.34 eV above  $E_C$ ) is quantitatively agreeing with the experimental result of  $\sim 0.4$  eV above



**Fig. 3.** (a)  $V_T$ , (b) SS, (c)  $g_m$ , (d)  $\mu_{FE}$  scaling metrics of ITO transistors with In:Sn ratio of 9:1, 6:1, 3:1,  $L_{ch}$  from 60 nm to 1  $\mu\text{m}$  and pure  $\text{In}_2\text{O}_3$  transistors as a comparison group.  $T_{ch}$  of ITO transistors with In:Sn ratio of 9:1, 6:1, and  $\text{In}_2\text{O}_3$  transistors is 2.1 nm.  $T_{ch}$  of ITO transistors with In:Sn ratio of 3:1 is 2.3 nm. Each data point represents the average of at least three devices.



**Fig. 4.** Atomic structures of (a)  $\text{In}_2\text{O}_3$  and (b)  $\text{SnO}_2$  used for CNL and band alignment calculation. Band structures of (c)  $\text{In}_2\text{O}_3$  and (d)  $\text{SnO}_2$ . The calculated CNL of  $\text{In}_2\text{O}_3$  lies  $\sim 0.34$  eV above CBE, while CNL of  $\text{SnO}_2$  lies  $\sim 0.24$  eV above CBE. CNLs are used for band alignment between  $\text{In}_2\text{O}_3$  and  $\text{SnO}_2$ . The band edges are rigidly shifted to reproduce the experimental band gaps.

$E_C$  [24]. In this band alignment, the conduction band of  $\text{SnO}_2$  is  $\sim 0.1$  eV above that of  $\text{In}_2\text{O}_3$ , so electrons will accumulate in the  $\text{In}_2\text{O}_3$  region in the  $\text{In}_2\text{O}_3$ - $\text{SnO}_2$  composite films. As a result,  $\text{In}_2\text{O}_3$  would act as the main electron-conducting channel while  $\text{SnO}_2$  behaves as the weak potential barrier in the ITO film against electron transport. Therefore, higher Sn concentration will reduce the electron transport through the  $\text{In}_2\text{O}_3$  conduction pathway and lead to poorer device performance including larger SS and lower  $\mu_{FE}$ .

Fig. 5(a) and (b) present the typical transfer and output characteristics of an ITO transistor with In:Sn ratio of 9:1,  $L_{ch}$  of 60 nm, and  $T_{ch}$  of 2.1 nm after 300  $^\circ\text{C}$  annealing in  $\text{O}_2$  for 60 s. An on/off ratio of  $3.3 \times 10^7$  and a positive  $V_T$  of 0.33 V are achieved at  $V_{DS}$  of 0.1 V, indicating an enhancement-mode operation by definition. Such positive  $V_T$  shift can be understood by the filling of the existing oxygen vacancies in ALD ITO films. It is known that oxygen vacancies

act as shallow donors in doped  $\text{In}_2\text{O}_3$ , which accounts for the Fermi level pinned deeply in the conduction band [15], [25]. A previous study has reported the carrier density in pulsed laser deposited ITO film can be adjusted by  $\text{O}_2$  pressure during growth [26]. Similarly, oxygen atoms induced during  $\text{O}_2$  annealing can also fill oxygen vacancies, lower the electron density, and bring down the Fermi level. Fig. 5(c) and (d) show the transfer and output characteristics of an ITO transistor with In:Sn ratio of 9:1,  $L_{\text{ch}}$  of 1  $\mu\text{m}$  and  $T_{\text{ch}}$  of 2.1 nm after 300  $^\circ\text{C}$  annealing in  $\text{O}_2$  for 60 s. The hysteresis is significantly reduced to 0.02 V compared to devices without annealing, suggesting  $\text{O}_2$  annealing helps eliminate the traps at the  $\text{In}_2\text{O}_3/\text{SnO}_2$  interfaces in the alloy ITO film. There is no obvious improvement in device performance by increasing  $\text{O}_2$  annealing time. Fig. 5(e)–(h) presents the transfer and output characteristics of ITO transistors with In:Sn ratio of 9:1,  $L_{\text{ch}}$  of 60 nm and 1  $\mu\text{m}$ , respectively,  $T_{\text{ch}}$  of 2.1 nm after 300  $^\circ\text{C}$  annealing in FG for 60 s. Compared to as-fabricated devices, FG annealing at 300  $^\circ\text{C}$  slightly shifts the  $V_T$  negatively and has a limited effect to improve the  $\text{In}_2\text{O}_3/\text{SnO}_2$  interface quality. FG annealing effect here is similar to other reported work on ternary or quaternary oxide semiconductors and in great contrast to ALD  $\text{In}_2\text{O}_3$  film [13].

Fig. 6 summarizes the scaling metrics of ITO transistors with In:Sn ratio of 9:1, 6:1, 3:1, and  $L_{\text{ch}}$  from 60 nm to 1  $\mu\text{m}$  after  $\text{O}_2$  and FG annealing at 250  $^\circ\text{C}$  and 300  $^\circ\text{C}$  for 60 s compared to devices without annealing. Fig. 6(a) compares  $V_T$  of ITO transistors with In:Sn ratio of 9:1 under different annealing conditions. A large positive  $V_T$  shift is observed in all  $\text{O}_2$  annealed ITO transistors due to the filling of oxygen vacancies and likely also the reduction of defects induced in fabrication [13], [27]. Besides,  $\text{O}_2$  annealing also weakens the  $L_{\text{ch}}$  dependent  $V_T$ . Fig. 6(b) and (d) show SS and  $\mu_{\text{FE}}$  versus  $L_{\text{ch}}$  characteristics of ITO transistors with In:Sn ratio of 9:1 under different annealing conditions. A minimum SS of 80 mV/dec and a maximum  $\mu_{\text{FE}}$  of 28  $\text{cm}^2/\text{V}\cdot\text{s}$  are achieved after  $\text{O}_2$  annealing, which is comparable to other amorphous oxide semiconductor TFTs. Similar phenomena are also observed in ITO transistors with In:Sn ratio of 6:1 and 3:1 as shown in Fig. 6(e)–(l). Therefore,  $\text{O}_2$  can be considered as a better choice to passivate the interface traps and improve device electrical performance in low-temperature annealing process [13], [27].

In addition, bias instability of ALD ITO transistors is also studied. Fig. 7(a) and (b) demonstrate the evolution of transfer characteristics of ITO transistors with In:Sn ratio of 9:1,  $L_{\text{ch}}$  of 60 nm, and  $T_{\text{ch}}$  of 2.1 nm under gate bias of  $-3$  and 3 V, respectively, for a stress time up to 2000 s. Fig. 7(c) and (d) show  $-\Delta V_T$  versus time of ITO transistors with In:Sn ratio of 9:1,  $L_{\text{ch}}$  of 60 nm and 1  $\mu\text{m}$ . A negative  $V_T$  shift is observed in both cases under gate bias of  $-3$  and 3 V, which is different from indium-gallium-tin-oxide (IGZO) TFTs where positive  $V_T$  shift is observed resulting from the charge trapping of accumulated electrons [28], [29]. Such a phenomenon can be explained by introducing the TNL model [30]. According to the previous calculation, TNL is located  $\sim 0.32$  eV above the conduction band in ultrathin  $\text{In}_2\text{O}_3$  [31]. Because of the similarity of ALD  $\text{In}_2\text{O}_3$  and ALD ITO, it can be assumed

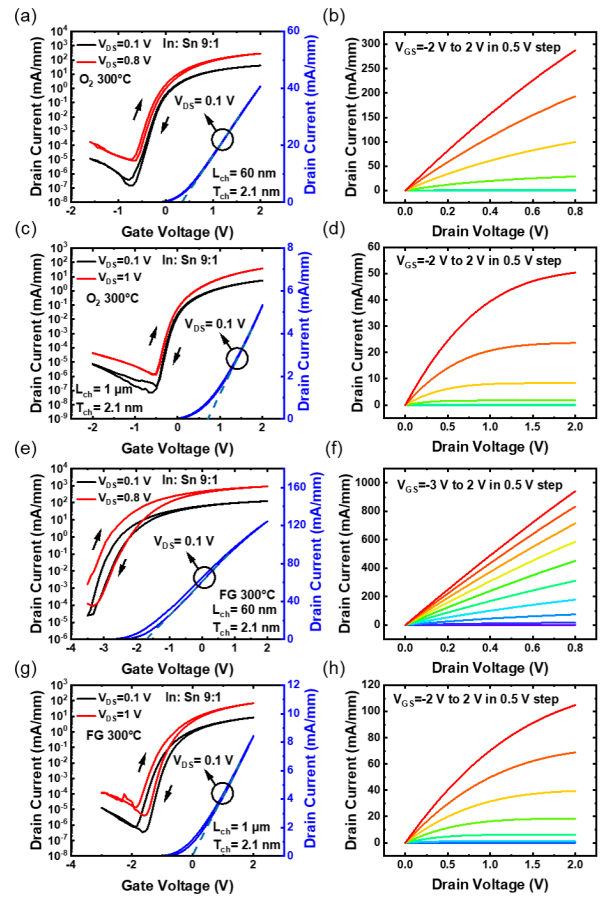


Fig. 5. (a) Transfer and (b) output characteristics of an ITO transistor with In:Sn ratio of 9:1,  $L_{\text{ch}}$  of 60 nm and  $T_{\text{ch}}$  of 2.1 nm after 60 s  $\text{O}_2$  annealing at 300  $^\circ\text{C}$ . (c) Transfer and (d) output characteristics of an ITO transistor with In:Sn ratio of 9:1,  $L_{\text{ch}}$  of 1  $\mu\text{m}$  and  $T_{\text{ch}}$  of 2.1 nm after 60 s  $\text{O}_2$  annealing at 300  $^\circ\text{C}$ . (e) Transfer and (f) output characteristics of an ITO transistor with In:Sn ratio of 9:1,  $L_{\text{ch}}$  of 60 nm after 60 s FG annealing at 300  $^\circ\text{C}$ . (g) Transfer and (h) output characteristics of an ITO transistor with In:Sn ratio of 9:1,  $L_{\text{ch}}$  of 1  $\mu\text{m}$  and  $T_{\text{ch}}$  of 2.1 nm after 60 s FG annealing at 300  $^\circ\text{C}$ .

that TNL in ITO is also likely to be deeply aligned in the conduction band due to its large density of valence band states [24], [32], [33]. Since the Fermi level is located below TNL, the donor-like interface states in between will always lead to a negative  $V_T$  shift regardless of the polarity of gate bias, similar to the observation in ALD  $\text{In}_2\text{O}_3$  [33]. Fig. 7(e) and (f) show  $-\Delta V_T$  as a function of stress time of ITO transistors with In:Sn ratio of 9:1,  $L_{\text{ch}}$  of 60 nm and 1  $\mu\text{m}$  after  $\text{O}_2$  annealing at 250  $^\circ\text{C}$  for 60 s. The  $L_{\text{ch}}$  dependent  $-\Delta V_T$  relation is nearly eliminated by the removal of defects after  $\text{O}_2$  annealing. Fig. 7(g) and (h) present  $-\Delta V_T$  as a function of stress time of ITO transistors with In:Sn ratio of 9:1 after FG annealing at 250  $^\circ\text{C}$  for 60 s. No big difference is observed between the results after FG annealing and as-fabricated ITO transistors, indicating ALD ITO films are more stable in FG compared to the serious hydrogen doping issue in IGZO [9], [34]. Reliability is one of the most important factors that need serious consideration in the development of a manufacturing technology. Despite the encouraging transistor characteristics of atomically thin ITO films demonstrated above, further experiments are still highly

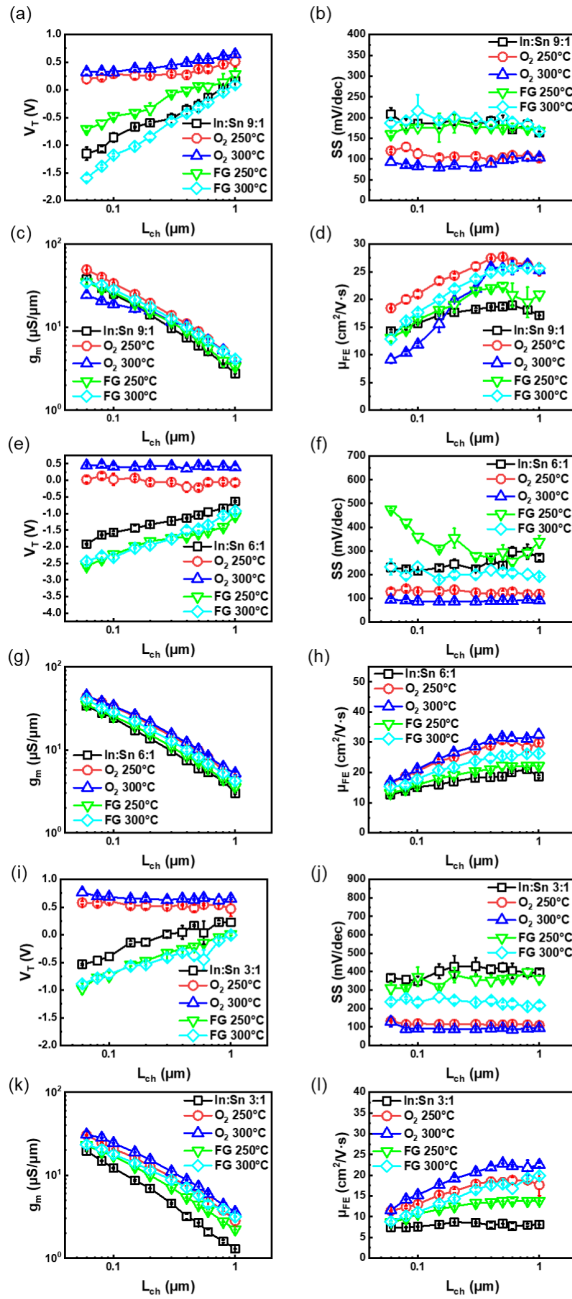


Fig. 6. (a)  $V_T$ , (b) SS, (c)  $g_m$ , (d)  $\mu_{FE}$  scaling metrics of ITO transistors with In:Sn ratio of 9:1,  $L_{ch}$  from 60 nm to 1  $\mu\text{m}$  and  $T_{ch}$  of 2.1 nm compared to the results after 60 s  $O_2$  and FG annealing at 250  $^\circ\text{C}$  and 300  $^\circ\text{C}$ . (e)  $V_T$ , (f) SS, (g)  $g_m$ , (h)  $\mu_{FE}$  scaling metrics of ITO transistors with In:Sn ratio of 6:1,  $L_{ch}$  from 1  $\mu\text{m}$  to 60 nm and  $T_{ch}$  of 2.1 nm under same annealing conditions. (i)  $V_T$ , (j) SS, (k)  $g_m$ , (l)  $\mu_{FE}$  scaling metrics of ITO transistors with In:Sn ratio of 3:1,  $L_{ch}$  from 60 nm to 1  $\mu\text{m}$  and  $T_{ch}$  of 2.3 nm under same annealing conditions.

demanded to improve the interface quality and reduce bias instability to meet the requirement for the application of ALD ITO as a BEOL-compatible transistor channel.

Fig. 8 presents a benchmark of ON-state current versus film thickness of recent ITO transistors deposited by ALD and sputtering. It can be seen that ALD deposited ITO films exhibit comparably high ON-state current as sputtered ITO films. Meanwhile, ALD has a more accurate control of the film thickness with high reproducibility and conformability

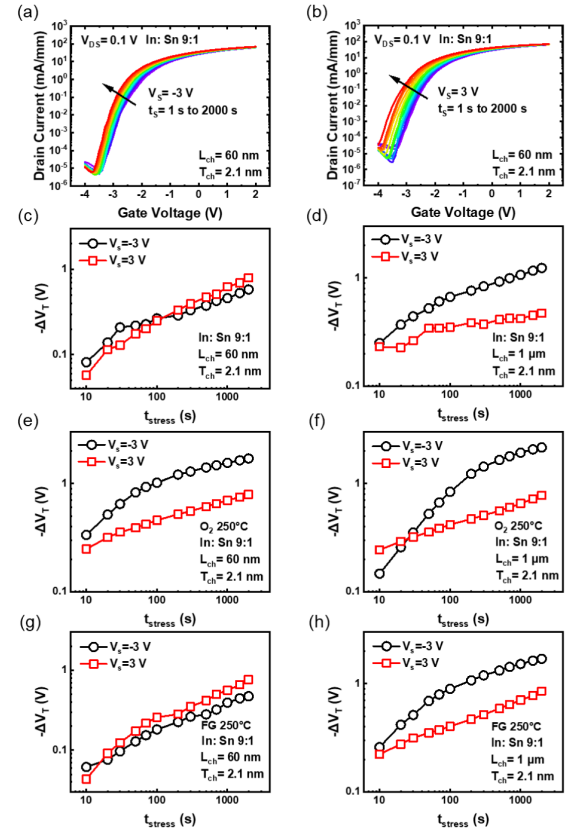


Fig. 7. Evolution of transfer characteristics of ITO transistors with In:Sn ratio of 9:1,  $L_{ch}$  of 60 nm, and  $T_{ch}$  of 2.1 nm under gate bias of (a)  $-3$  and (b)  $3$  V for a stress time of 2000 s. (c) and (d)  $V_{th}$  shift as a function of stress time of as-fabricated ITO transistors with In:Sn ratio of 9:1,  $T_{ch}$  of 2.1 nm,  $L_{ch}$  of 60 nm, and 1  $\mu\text{m}$  separately. (e) and (f)  $V_{th}$  shift as a function of stress time of ITO transistors with In:Sn ratio of 9:1,  $L_{ch}$  of 60 nm and 1  $\mu\text{m}$  after 60 s  $O_2$  annealing at 250  $^\circ\text{C}$ . (g) and (h)  $V_{th}$  shift as a function of stress time of ITO transistors with In:Sn ratio of 9:1,  $T_{ch}$  of 2.1 nm,  $L_{ch}$  of 60 nm and 1  $\mu\text{m}$  after 60 s FG annealing at 250  $^\circ\text{C}$ .

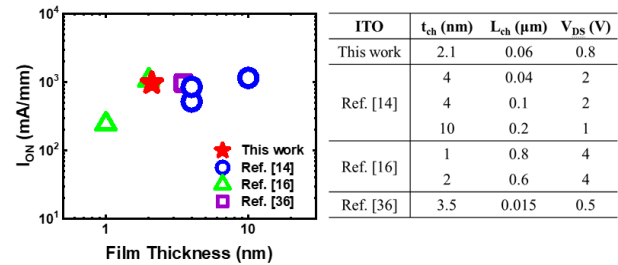


Fig. 8. Benchmark of ON-state current versus film thickness of recent ITO transistors. Solid symbol represents ITO films deposited by ALD and hollow symbols represent ITO films deposited by sputtering.

than sputtering, which paves way for further device scaling with high precision.

#### IV. CONCLUSION

In summary, atomically thin ITO transistors are demonstrated for the first time by the ALD process at 225  $^\circ\text{C}$ . A maximum ON-state current of 970 mA/mm at  $V_{DS}$  of 0.8 V and an on/off ratio up to  $10^7$  are achieved in ITO transistor with In:Sn ratio of 9:1,  $L_{ch}$  of 60 nm and  $T_{ch}$  of 2.1 nm. Comparison between ITO transistors with different In:Sn ratios reveals the effect of Sn concentration to impede the electron transport which is understood by DFT calculation of band

alignment of  $\text{In}_2\text{O}_3$  versus  $\text{SnO}_2$ . BEOL-compatible low-temperature annealing is also systematically studied. An SS as low as 80 mV and a  $\mu_{\text{FE}}$  of  $28 \text{ cm}^2/\text{V}\cdot\text{s}$  are achieved after  $\text{O}_2$  annealing due to the filling of oxygen vacancies and elimination of exhibiting defects. Finally, bias instability measurement shows a negative  $V_T$  shift for both positive and negative stress voltage, which is ascribed to the existence of donor-like interface states below TNL. This work provides prospects for the future application of ALD ITO films in monolithic 3-D integration.

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